CLAIMS

Please enter the following claims (claims 1-18)

1. (currently amended) A memory array that simultaneously reads and writes different addresses of the same memory array, comprising:

a plurality of memory cells arranged in two equally sized ~~arrays~~ blocks, each memory cell having a separate read and write port, wherein each port is coupled to a wordline that activates the memory cells, and a bitline that transfers data to or from said memory cells;

read bitlines and write bitlines respectively connected to a read and write port of each memory cell along a column of each of said ~~arrays~~ blocks;

read wordlines and write wordlines respectively connected to the read and write ports of each memory cell along a row of each of said ~~arrays~~ blocks; ~~and~~

a row of differential sense amplifiers located between the two blocks wherein one sense amplifier is provided for each column of said ~~arrays~~ blocks, and wherein each bitline from the first block ~~array~~ being respectively attached to a first input terminal of the corresponding differential sense amplifier, and each read bitline from the second block ~~array~~ being respectively attached to a second input terminal of the corresponding differential sense amplifier; each write bitline in the first block connecting to the write bitline in the second block in the same column, enabling a simultaneous read and write by activating the read wordline from the first block, the write wordline from either the first or the second block, and the write bitlines traversing both blocks, said arrangement resulting in transforming noise coupling from the write bitline to the read bitlines into common mode noise that is rejected by said differential sense amplifiers, and

a means for driving a write bitline in said first block and a write bitline in said second block in the same direction to create said common mode noise in a read bitline in said first block and a read bitline in said second block.

2. (currently amended) The memory array of claim 1 wherein a row of reference cells in each of said two blocks is connected to a reference wordline and to said read bitlines, and wherein when said reference wordline is activated, said read bitline coupled to said activated reference cell discharges to a voltage level that is mid-way between the value at which a cell stores a logic 0 and a logic 1, enabling a simultaneous read and write operation by activating said read wordline from said first block, said reference cell wordline from said second block and said write wordline from said first or said second block and said write bitlines traversing both blocks, resulting in an arrangement for transforming the noise coupling said write bitline to said read bitlines into said common mode noise that is rejected by said differential sense amplifiers. ~~each write bitline in the first array is connected to the write bitline in the second array in the same column, enabling simultaneous read and write by activating the read wordline from the first array, the reference wordline from the second array, the write wordline from either the first or the second array and the write bitlines traversing both arrays, said arrangement resulting in transforming noise coupling from the write bitline to the read bitline into common mode noise that is rejected by said differential sense amplifiers~~

3. (currently amended) The memory array of claim 1 wherein a write bitline in the first ~~array~~ block and in the second array block are respectively driven by a first and second driver having the same slew characteristics, said first and second drivers switching simultaneously.

4. (currently amended) A memory array of memory cells, each cell provided with separate read and write ports, comprising:

read and write wordlines coupling memory cells along each row of the array, read bitlines and write bitlines coupling cells along each column of the array, and differential read sense amplifiers arranged in a separate row of the array;

~~a read bitline pair with one read line connecting one terminal of a differential sense amplifier to a first half of the cells along a column of the array, and a second read bitline connecting the second half of the cells along the same column of the array;~~

~~a first row of reference cells connected to the first read bitline segments and a second row~~

~~of reference cells connected to the second bitline segments;~~

~~a first segment of a re-entrant read bitline linking a complementary input of the differential sense amplifier to a segment of the read bitline for each column; and~~

~~a second segment of the re-entrant read bitline linking the second segment of the read bitline and extending over the first section of the array arranged symmetrically about a horizontal line at the center of the array to the second segment of the re-entrant bitline, wherein a simultaneous read and write operation is achieved by activating a read wordline in the first section of the array connected to the first bitline segment, a reference wordline in the second portion of the array, a write wordline in the first or the second section of the array and all the write bitlines and all the differential sense amplifiers~~

said memory array being divided into two equally sized blocks with each column thereof divided into two segments, and configured with a row of sense amplifiers located above or below the two blocks;

a read bitline and a write bitline connected to read and write ports respectively of memory cells in each column of each of said blocks, wherein respective read or write bitlines in one of said blocks use the same conductor level as the respective read and write bitlines in said second block;

an additional conductor forming a re-entrant bitline connected to the read bitline in said first block extending across said second block without connecting to cells in said second block for each column, and an additional re-entrant bitline connected to the read bitline in said second block extending across said first block without connecting to cells in said first block for each column;

a connection from one re-entrant bitline extending from said first block to a terminal of said differential sense amplifier located adjacent to said first block at an edge of said first block opposite to said second block for each column of said array;

a connection from the read bitline in said first block to a second terminal of said differential amplifier in each column in said array;

a connection between the write bitline in said first block to the write bitline in said second block for each column in said array,

wherein the read bitlines and the re-entrant bitlines are placed on separate layers of connectivity, and

wherein a voltage swing on the write bitline couples an equivalent noise into the read bitline segments connected to the first terminal of said differential amplifier, and the read bitline segment connected to the second terminal of said differential amplifier for each column, ~~thus~~ transforming the noise into said a common mode noise which is rejected by said differential sense amplifiers.

5. (currently amended) The memory array of claim 4 wherein a row of reference cells in each of said two blocks connected to a reference wordline and the read bitlines, wherein when the reference wordline is activated, the read bitline coupled to the activated reference cell discharges to a voltage level that is mid-way the value at which a cell stores a logic 0 and a logic 1 enabling simultaneous read and write by activating the read wordline from the first block, the reference cell wordline from the second block and the write wordline from either the first or the second block and the write bitlines traversing both blocks, said arrangement resulting in transforming noise coupling from the write bitline to the read bitlines into common mode noise that is rejected by said differential sense amplifiers. ~~said first and second sections of the array have each the first and the second segments of said re-entrant read bitlines for each column of memory array~~.

6. (original) The memory array of claim 4 wherein the write bitlines are driven by a row of write bitline drivers located along the periphery of the array.

7. (original) The memory array of claim 4 wherein the write bitlines are driven by a row of write bitline drivers located at both the first and second edges of the array, with a first plurality of write bitlines connected to the first edge drivers and the remaining to the second edge drivers.

8. (currently amended) The memory array of claim 4, wherein ~~the read bitlines and the re-entrant bitlines are placed on separate layers~~ each block is divided into an even number of sub-blocks, where each column of each sub-block has a read bitline connected to said memory cells in said sub-block, one write bitline connected to said memory cells of said sub-block and a re-entrant read bitline running across said sub-block without connecting to the memory cells in said sub-block, and wherein read bitlines in one sub-block connect to the re-entrant read bitlines of a corresponding column in adjacent sub-blocks.

9. (original) The memory array of claim 4 wherein the write bitlines are on the same layer of connectivity as the read bitlines

10. (original) The memory array of claim 4 wherein the write bitlines are on the same layer of connectivity as the re-entrant bitlines

11. (original) The memory array of claim 4 wherein the write bitlines are on a layer of connectivity which is different from either the read bitlines or the re-entrant bitlines.

12. (currently amended) A memory array of dual port memory cells arranged in an array formation comprising:

memory cells in a row of said array connected to read wordlines and write wordlines, said memory cells along a column being connected by a read bitline;

an arrangement of differential sense amplifiers having each an input thereof connected to a reference voltage, the read bitline connecting all the memory cells along one column of the array to the second input of corresponding differential sense amplifier;

a write bitline provided with re-entrant connections, wherein a first segment of a write bitline is connected to half the cells along a column of the array, and a second segment of the write bitline is connected to the remaining cells along the same column of the array;

a write driver connected to and driving the first write bitline segment, and a second write driver connected to and driving the second write bitline segment; and

input circuitry linking the write drivers, each driver simultaneously driving ~~to and~~ from and to opposite state at a given slew rate,

wherein the re-entrant connections link a write bitline driver to the write bitline in one block, and a second write bitline driver to the write bitline in a second block, such that one-half the cells in each column are coupled to the first driver, and the remaining cells are coupled to the second driver; and wherein the read bitline from one block is connected to the read bitline in the second block and is also connected to the input of a sense amplifier for each column and wherein simultaneous read and write operations are realized by activating one read wordline, one write wordline, the sense amplifiers and all the write bitline drivers, wherein the write bitline drivers operate for each column in a way that the output voltage of the first driver is of the same magnitude and 180° out-of-phase from the output voltage of the second driver, and wherein when the voltage on the write bitline changes, no noise is coupled from the write bitlines to the read bitlines.

13. (original) The memory array of claim 12 wherein true and complement write drivers are positioned at opposite ends of the array and the arrangement of differential sense amplifiers is placed at the periphery of said array.

14. (canceled)

15. (original) The memory array of claim 14, wherein the re-entrant connections are positioned in a connecting layer that coincides with that of the read bitlines.

16. (original) The memory array of claim 14, wherein the write bitline connections are positioned in a connecting layer that coincides with that of the read bitlines

17. (original) The memory array of claim14, wherein the read bitlines connections are

positioned in a connecting layer that differs from that of the re-entrant or the write bitlines.

18. (original) The memory array of claim 14, wherein a plurality of pairs of true and complement write drivers are located on one side of said array, and the remaining pairs of true and complement drivers are located on a second side of said array.

19. (new) The memory array of claim 14 wherein each block is divided into an even number of sub-blocks, where each column of each sub-block has one read bitline connected to said memory cells in said sub-block, one write bitline connected to said memory cells of said sub-block and a re-entrant write bitline running across said sub-block without connecting to the memory cells in said sub-block; and wherein write bitlines in one sub-block connect to the re-entrant write bitlines of a corresponding column in adjacent sub-blocks.